M206

PLL TV MICROCOMPUTER INTERFACE

- HIGHLY INTEGRATED SOLUTION INCLUDING PLL SYNTHESIZER, NV MEMORY, D/A CONVERTERS, BAND SELECT OUTPUTS, CLOCK OSCILLATOR, IR SIGNAL PRE-PROCESSOR AND SERIAL BUS INTERFACE
- 32 x 16 BITS OF NV MEMORY WITH LIFETIMES OF 10^4 CYCLES/WORD AND MINIMUM 10 YEARS RETENTION STORES TUNING DATA FOR 30 CHANNELS PLUS PRESET VALUES FOR THE SIX ANALOG OUTPUTS
- PRE-PROCESSOR FOR INFRARED REMOTE CONTROL SIGNALS REDUCES COMPONENT COUNT
- SIX PWM D/A CONVERTERS WITH 64-STEP RESOLUTION
- FOUR OPEN-DRAIN BAND SELECT OUTPUTS RATED TO 13.2 V
- ON-CHIP 4 MHz CLOCK OSCILLATOR WITH BUFFERED OUTPUT
- INTEGRATED DIGITAL POWER-ON RESET
- 3-WIRE SERIAL BUS TO LOAD/READ INTERNAL REGISTERS

DESCRIPTION

The M206 is a highly integrated, programmable LSI integrated circuit for microcomputer controlled TV applications, realized using an advanced N-channel double polysilicon gate technology (NVMOS) that allows the integration of non-volatile memory and standard logic on the same chip.

It contains a phase-locked loop (PLL) synthesizer, six pulse-width modulation (PWM) digital/analog converters, a four-bit parallel output buffer, clock oscillator with buffered output, pre-processor for infrared remote control signals and a 3-wire serial bus interface.

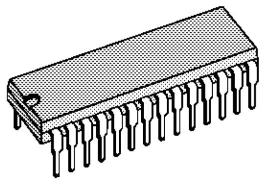
The M206 interfaces with a microcomputer through the three-wire serial bus and is programmed by loading thirteen internal registers - twelve of which are readable to simplify programming.

The PLL synthesizer requires an external 64 + 15/16 prescaler and divider and works with a phase comparator reference frequency of 0.9765 kHz. Outputs are provided to control the division ratio of the prescaler and to signal the out-of-lock condition to the microcomputer.

The infrared remote control signal pre-processor consists of a preamplifier, a squarer and a digital filter to separate noise from signals transmitted by the M708, M709 and M710 remote control transmitters. The output of this pre-processor is connected to the interrupt input of a microcomputer programmed to receive and decode the signal.

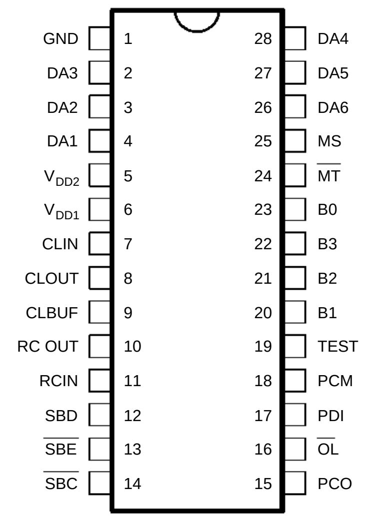
The M206 is supplied with two separate 5 V supply inputs, each provided with internal power-on reset circuits. The first, V_{DD1}, supplies the remote control and clock circuits in both standby and TV set operation. The second, V_{DD2}, supplies the rest of the circuits and is only active during TV operation.

The M206 is packaged in a 28-pin dual in-line plastic package.



DIP28
(Plastic Package)
ORDER CODE : M206B1

PIN CONNECTIONS

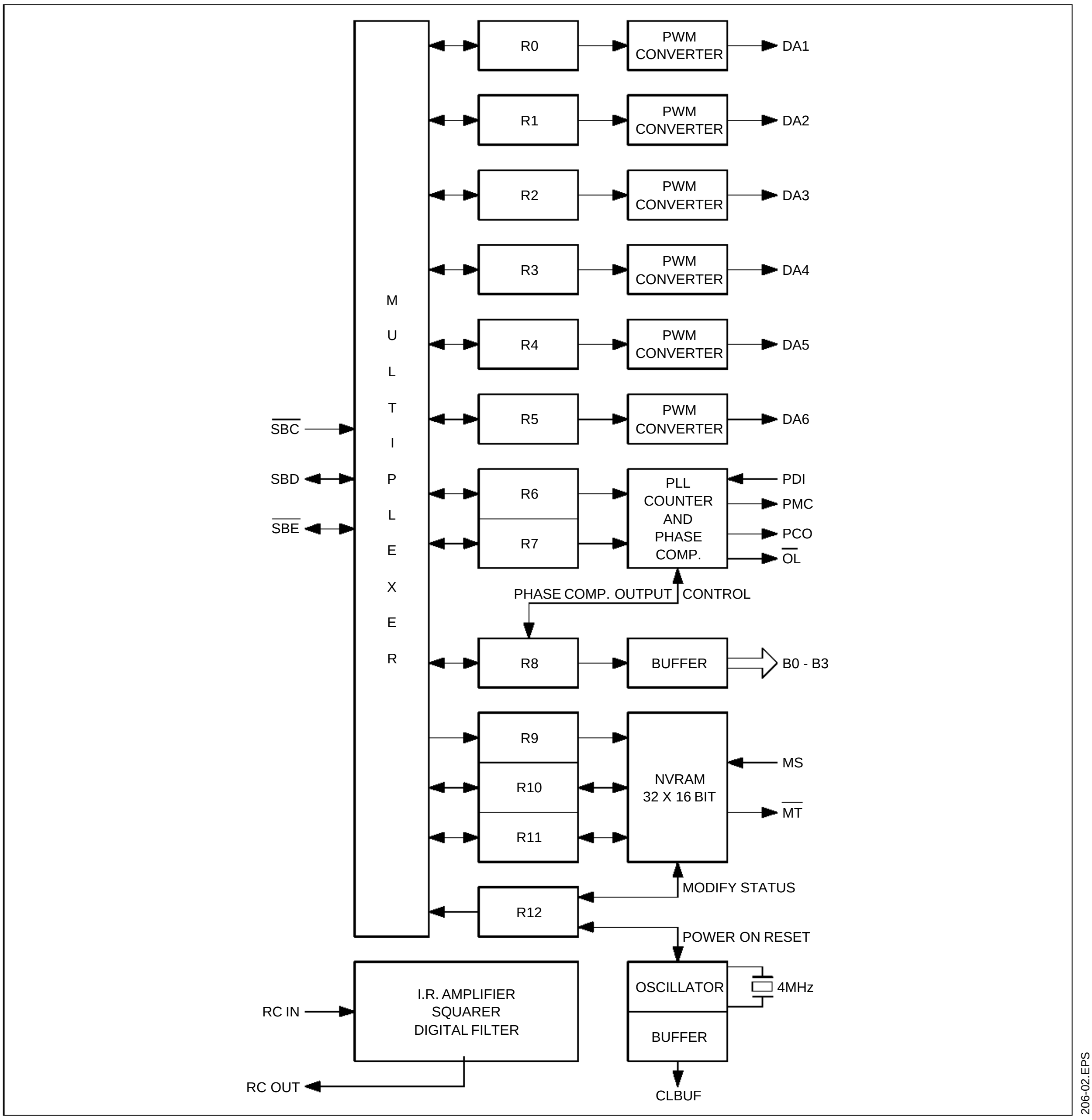


PIN DESCRIPTION

Pin Number	Symbol	Function
2-3-4-28-27-26	DA1 to DA6	*Digital/Analog converter outputs (open-drain outputs)* Output from the six pulse-width modulation D/A converters.
23-22-21-20	B0 to B3	*Band drive outputs (open-drain outputs)* Outputs from the four-bit buffer used for band selection.
12	SBD	*Serial Bus Data (bidirectional)* Data line for serial communication with a microcomputer.
13	$\overline{SBE}$	*Serial Bus Enable (bidirectional, active low)* Enables serial bus transmissions.
14	$\overline{SBC}$	*Serial Bus Clock (input, active low)* Clock for serial bus transmissions.
11	RCIN	*Remote Control signal Input (analog input)* Input to the infrared remote control signal preprocessor. Connected to the output of the IR preamplifier. Minimum input level 0.5 V peak-to-peak.
10	RCOUT	*Remote Control signal Output* Output from the infrared remote control signal pre-processor. To be connected to the interrupt input of a microcomputer.
17	PDI	*Programmable Divider Input (input)* This pin is the input of the programmable divider and is connected to the output of the prescaler.
18	PCM	*Prescaler Modulo Control (output)* Control signal to set the prescaler division ratio (15 if high, 16 if low).
16	$\overline{OL}$	*Out of Lock (output, active low)* Signals an out of lock condition. This output is also active during the power on reset sequence.
15	PCO	*Phase Comparator Output* The output of the phase comparator. Connected to the input of a low pass filter used to generate the tuning voltage.
19	TEST	*Test pin (input)* The test pin is used only to test the device and is not specified for customer use. It must be connected to ground.
7-8	CLIN-CLOUT	*Clock oscillator connections* A 4 MHz quartz crystal is connected between these pins.
6-5-1	V_{DD1}-V_{DD2}-GND	*Power Supply Connections* V_{DD1} is the + 5 V standby supply input ; V_{DD2} is the main + 5 V supply input.
25	MS	*Memory Supply Input (input)* Programming pulses for the NV memory are supplied to this pin during store cycles.
24	$\overline{MT}$	*Memory Timing (output, active low)* This output supplies the timing for the memory write pulses supplied to the MS input during store cycles.
9	CLBUF	*Clock Buffer (output)* This is a buffered output from the on-chip clock oscillator and can be used to drive other components (for example the microcomputer)

206-01.TBL

BLOCK DIAGRAM

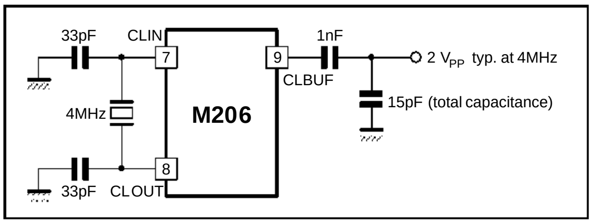


FUNCTIONAL DESCRIPTION

Clock (see Figure 1)

To use the internal oscillator a 4MHz quartz crystal is connected between the pins CLIN and CLOUT. If an external clock is used this must be connected to CLIN and CLOUT left unconnected or, if required as a clock output, loaded by a capacitor up to 15pF. The minimum external clock amplitude is 2V peak-to-peak. A buffered clock output, CLBUF, is provided which can drive up to three ± 100µA loads.

Figure 1



Loading And Reading Internal Registers

The M206 is programmed by loading a set of internal registers through a 3-wire serial bus. The functions of these registers are summarised in Table 1.

The 3-wire serial bus consists of the signals SBD (Serial Bus Data), $\overline{SBE}$ (Serial Bus Enable) and SBC (Serial Bus Clock). The enable and data pins, SBD and $\overline{SBE}$, are bidirectional.

Data is accepted when the clock is low (active) and latched into the M206 on the low-high transition of the clock. All bus transfers are controlled by $\overline{SBE}$.

Register Loading

Serial data transferred from the microprocessor to the M206 has the following format : see Figure 2 and Table 2.

Table 2

Bit	Description
CS	Chip Select (always low)
PARITY	Parity bit (the number of " H " bits transmitted is odd)
R/W	Read/Write. High for Register Load ; Low for Register Read
A0-A3	Register Address (see Table 1)
D0-D7	Data to be loaded into register (load operation only)

206-03.TBL

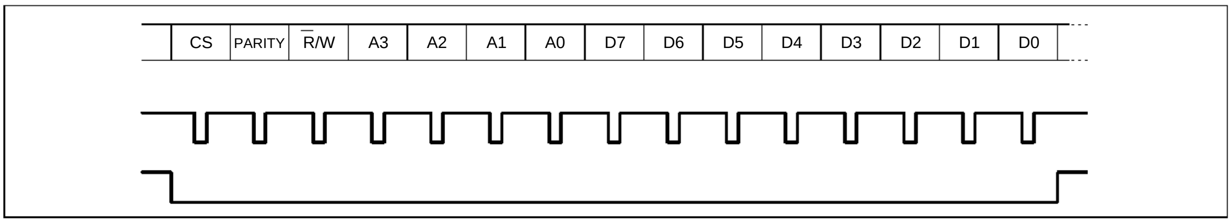
The received data word is checked - length, CS and parity - immediately after the low-high transition of SBE. If the received word is valid this is signalled to the microprocessor by forcing the SBE line low for 20-24µs (see Figure 3).

Table 1 : Summary of Internal Registers

Register Number	Address				Number of Bits	Function
	A3	A2	A1	A0		
0	L	L	L	L	6	D/A Converter n° 1
1	L	L	L	H	6	D/A Converter n° 2
2	L	L	H	L	6	D/A Converter n° 3
3	L	L	H	H	6	D/A Converter n° 4
4	L	H	L	L	6	D/A Converter n° 5
5	L	H	L	H	6	D/A Converter n° 6
6	L	H	H	L	7	PLL Counter (MSB)
7	L	H	H	H	8	PLL Counter (LSB)
8	H	L	L	L	7	Buffer Outputs/Phase Comp. Output Control
9	H	L	L	H	5	NV Memory Address
10	H	L	H	H	8	NV Memory DATA
11	H	L	H	H	8	NV Memory DATA
12	H	H	L	L	2	NV Memory Modify Control/Reset Control

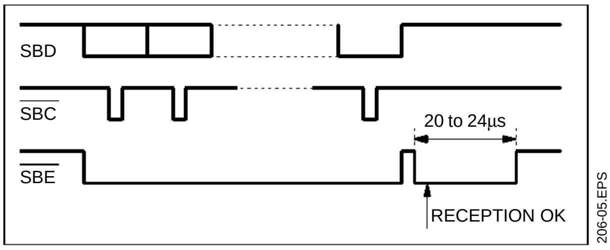
206-02.TBL

Figure 2



FUNCTIONAL DESCRIPTION (continued)

Figure 3



Register Reading

M206 registers are read by transmitting a 15-bit word as shown in Figure 4 with R/W low and the address of the register to be read in A0, A1, A2, A3. Bits D0-D7 can be high or low except when register 9 is addressed.

If this word is received correctly the $\overline{SBE}$ line is immediately pulled low by the M206 and after 24µs the contents of the addressed register will be available to be read (see Figure 4). The microprocessor reads this data by sending eight clock pulses. Data is output on the low-high transition of SBC and the first data bit is available before the first clock pulse.

Loading the Non-volatile Memory

Data is stored in the 32 x 16-bit NV memory by loading the new contents into registers 10 and 11 then the address into register 9. The memory modify cycle begins when the address has been loaded and successful completion is indicated by a logic ”1” in bit zero of register 12.

The time for a modify cycle varies from a few milliseconds to several hundred milliseconds during the device lifetime and is not internally limited. The storage operation should be aborted after one second if it proves unsuccessful. This is done by setting bit zero of register 12.

Reading the Non-volatile Memory

The NV memory is read by loading the address into register 9. The contents of the addressed word are automatically loaded into registers 10 and 11 and can be read by two register read operations. The data is ready 200µs after the address load.

PLL Counter

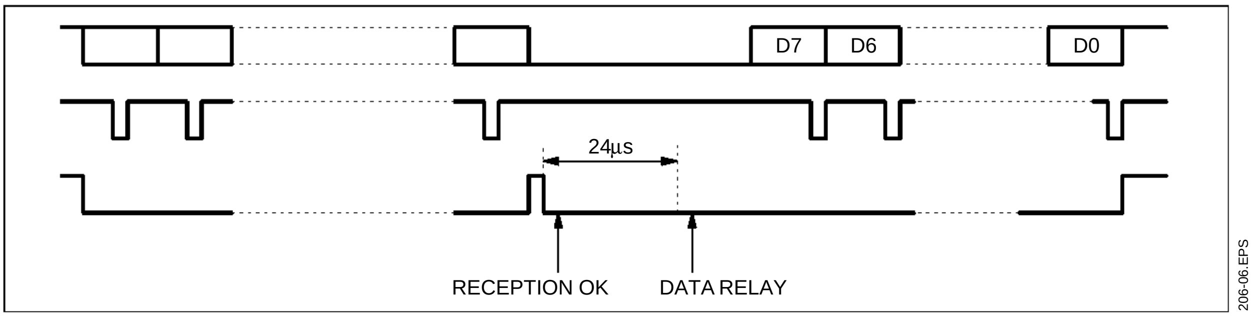
The PLL counter consists of a single counter that acts as the program counter (11-bit) and is swallow counter (4-bit) alternately. Data for the PLL counter is loaded into registers 6 and 7. Register 6 must be loaded first because the register 7 load operation initiates the data transfer to the PLL counter.

The reference frequency is produced by dividing the clock frequency by 4096. With a 4MHz clock this gives a reference frequency of 976.5Hz.

An out-of-lock signal is generated (output $\overline{OL}$) when the phase error between the reference frequency and the input frequency exceeds 0.72 (2µs).

The phase comparator output, PCO, has a three-state push pull configuration with a high level of 5V and a low level of 0V (with zero current sink or pump). The output impedance (both states) is typically 200Ω (400Ω maximum). The phase comparator output can be set to a high impedance state (both sink and pump transistors off) by setting bit 4 of register 8. The output is held in the high impedance state until this bit is reset. The phase comparator output should be set to high impedance when changing band.

Figure 4



FUNCTIONAL DESCRIPTION (continued)

Recovering Lock

The phase comparator output can also be set to high and low levels to restore normal operation when the oscillator stops or the prescaler functions incorrectly at high frequency.
In the first condition (oscillator off) the prescaler sometimes oscillates, at high frequency. The loop reacts by reducing the varicap voltage in an attempt to reduce the frequency, thus worsening the situation. This out-of-lock condition is signalled to the microprocessor (by the $\overline{OL}$ output) which can set the phase comparator output to low level, forcing the varicap voltage up and restarting the oscillator. The phase comparator output is forced low by setting bit 5 of register 8. After about 1ms this bit is automatically reset and the loop should lock again.
When the out-of-lock condition is caused by a failure of the prescaler to operate correctly at high frequencies the loop reacts by increasing the voltage, hence the frequency, again worsening the situation. To recover from this condition the phase comparator output is set high. This is done by setting bit 6 of register 8 which, as in the previous case, resets itself after 1ms.
The out-of-lock condition could also be caused by unwanted changes in band or PLL counter contents provoked by external interference (spikes on supply etc.). For this reason it is always advisable to reload the band and PLL counter registers before attempting to recover lock as described above. If the phase comparator output is in the high impedance state, the $\overline{OL}$ output signals the reset condition but not the out-of-lock condition.

Calculating PLL Counter Values

a) f = video carrier
b) IF = 38.9MHz
c) The frequency to be synthesized is f_S = f + IF
d) The Ref. frequency of the phase comparator is

$$f_{ref} = \frac{4.000\text{MHz}}{4096} = 0.97656\text{kHz}$$

e) Using the prescaler 64 + 15/16 the minimum frequency steps is f_{ref} x 64 = 62.5kHz
f) The modulo of division N is given by the ratio between the frequency to be synthesized and the reference frequency multiplied by 64. The result has to be rounded.

$$NS = \text{Integer rounded}\left[\frac{f_S}{f_{ref} \cdot 64}\right]$$

g) With the 64 + 15/16 prescaler and the particular counter of the M206 the division by N is given by $N_S = (I_S + 1) \cdot 15 + (R_S + 1) \cdot 16$
where I (integer part) controls the division by 15 (program counter) and R (rest) controls the division by 16 (swallow counter).
For ease of calculation we decrement N_S by one getting $N_C = N_S - 1$.
The numbers I_C and R_C are given by :
$N_C = (I_C + 1) \cdot 15 + (R_C + 1) \cdot 16$
$N_C - 31 = I_C \cdot 15 + R_C \cdot 16$
using the formulas :

$$R_C = N_C \pm 31 \pm 15 \cdot \text{Integer}\left[\frac{N_C \pm 31}{15}\right]$$

$$I_C = \frac{N_C \pm 31 \pm R_C \cdot 16}{15}$$

$R_S = R_C + 1$
$I_S = I_C \ 1$

Example :
Channel 21, f = 471.25MHz

f_S = f + IF, f_S = 471.25 + 38.9 = 510.15MHz

$$N_S = \text{Integer rounded}\left[\frac{510.15 \cdot 10^6}{62.5 \cdot 10^3}\right]$$

= Integer rounded [8162.4] = 8162

$N_C = N_S - 1 = 8161$

$$R_C = N_C - 31 - 15 \cdot \text{Integer}\left[\frac{N_C \pm 31}{15}\right]$$

$$= 8161 - 31 - 15 \cdot \text{Integer}\left[\frac{8161 \pm 31}{15}\right]$$

= 8130 - 15 · Integer [542]

= 8130 - 15 · 542 = 8130 - 8130 = 0

$$I_C = \frac{N_C \pm 31 \pm R_C \cdot 16}{15} = \frac{8161 \pm 31}{15} = 542$$

$R_S = R_C + 1 = 0 + 1 = 1$
$I_S = I_C - 1 = 542 - 1 = 541$

R and I have to be translated into binary code.

FUNCTIONAL DESCRIPTION (continued)

Digital/Analog Converters

The six pulse-width modulation (PWM) D/A converters have a resolution of 64 steps and an output frequency of 16kHz (with 4MHz clock).

At power on reset they are set to a duty cycle of zero.

Power On Reset

The V_{DD1} and V_{DD2} supplies have an integrated digital power on reset with a duration of 250ms.

The reset condition is signalled by a low level on the out-of-lock output, $\overline{OL}$. The microprocessor can test this condition by reading bit 1 of register 12. This bit is zero during power on reset and the $\overline{OL}$ output remains active until it is read. Reading this bit automatically restores it to a high state.

During power on reset time commands from the micoprocessor are not acknowledged. Power on reset also sets the phase comparator output to a high impedance, state. It is restored by resetting bit 4 of register 8.

Remote Control Signal Pre-processor

This section contains a preamplifier, squarer, digital filter and a pulse generator. The digital filter enables the pulse generator only if three successive negative going pulses (4 edges) are detected. The dis-tance between these pulses must be in the range 24-27µs (about 37-41kHz with a 4MHz clock). The input is not tested for the duration of the output pulse (192-256µs).
If this pre-processor is used in conjunction with M709 or M710 remote control transmitters valid signals can be recognized in the presence of extreme noise conditions. Separating the signals from the noise externally in this way reduces the number of interrupts that the microcomputer has to handle thus allowing it to concentrate on other takes. To take advantage of this section the M708, 709, 710 transmitters must operate with a clock frequency in the range 492-508kHz.
The input can be DC or AC compled to the I.R. preamplifier.
In case of DC coupling the quiescent input level is suggested to be 1.5V.

Figure 5

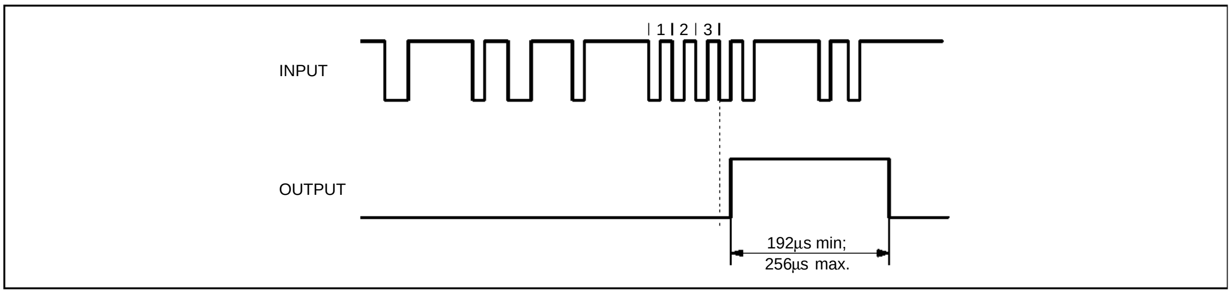
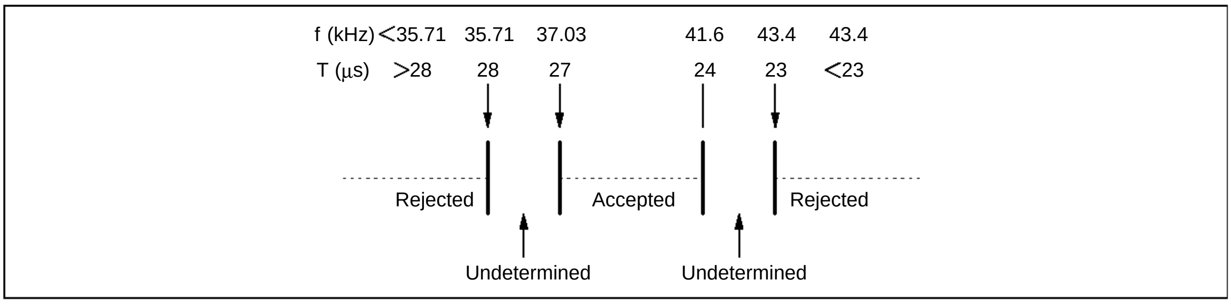


Figure 6 : Response of the Digital Filter as a Function of the Input Frequency (in kHz).



PROGRAMMING SUMMARY

Registers 0-5 : D/A Convertors 1-6

R0-R5 : 6 bits

5 (MSB)	0 (LSB)
BINARY CODED ANALOG VALUE	

Register 6 : PLL Program Counter

R6 : 7 bits

5 (MSB)	0
PROGRAM COUNT UPPER 7 BITS	

Register 7 : PLL Program/Swallow Counter

R7 : 8 bits

5	0 (LSB)
PROGR. COUNT LOWER 4 BITS	SWALLOW COUNT

Register 8 : Band Drive Outputs/Phase Comparator Output Control

6						0
PCOH	PCOL	PCOZ	B3	B2	B1	B0

B0-B3 Band drive outputs B0-B3
PCOZ Phase comparator output high impedance
PCOL Phase comparator output low level
PCOH Phase comparator output high level

PCOH	PCOL	PCOZ	Phase Comparator Output
L	L	L	Normal PLL Operation
L	L	H	High Impedance State
L	H	L	Low for 1ms then returns automatically to normal PLL operation
L	H	H	Low for 1ms then returns to high impedance state
H	L	L	High for 1ms then returns to normal PLL operation
H	L	H	High for 1ms then returns to high impedance
H	H	L	Normal Operation *
H	H	H	High Impedance *

* These combinations are not accepted and PCOL, PCOH are automatically reset low after 1ms.

Register 9 : NV Memory Address

R9 : 5 bits

4 (MSB)	0 (LSB)
ADDRESS	

Register 10 : NV Memory Data

R10 : 8 bits

7 (MSB)	0
UPPER EIGHT DATA BITS	

Register 11 : NV Memory Data

R11 : 8 bits

7	0 (LSB)
UPPER EIGHT DATA BITS	

Register 12 : NV Modify Status/Reset Status

R12 : 2 bits

1	0
RESET STATUS	MODIFY STATUS

Flag	L	H
MODIFY STATUS	Modify in progress.	Modify over.
RESET STATUS	Reset actived.	Reset not actived.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD1}, V_{DD2}	Supply Voltage		- 0.3, 7	V
V_{PP}	Memory Supply Voltage		- 0.3, 28	V
V_I	Input Voltage	(except Pin 11) Pin 11	- 0.3, 7 - 0.3, 15	V V
$V_{O\ (off)}$	Off State Output Voltage	(except Pins 2-3-4-26-27-28-20 to 24) Pins 2–3–4–20 to 23–26 to 28 Pin 24	7 15 28	V V V
I_{OL}	Output Current	(except Pins 2–3–4–26–27–28) Pins 2–3–4–26–27–28	5 10	mA mA
I_{OH}	Output Current (Pins 15, 9)		- 5	mA
P_{tot}	Total Package Power Dissipation		1	W
T_{stg}	Storage Temperature		- 25, 125	°C
T_{oper}	Operating Temperature		0, 70	°C

206-04.TBL

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70^{o}C ; typical values are at T_{amb} = 25^{o}C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage (Pin 5)		4.75	5	5.25	V
V_{DD2}	Supply Voltage (Pin 6)		4.75	5	5.25	V
V_{PP}	Memory Supply Voltage (Pin 25)		24	25	26	V
V_{IL}	Input Low Voltage (Pins 12-13-14-17)		0		0.8	V
V_{IH}	Input High Voltage (Pins 12-13-14-17)		2.4		5.25	V
V_{IPP}	Peak to Peak Signal (Pin 11)	AC Coupling	0.5		13.2	V
V_{TH}	Threshold Voltage (Pin 11)	DC Coupling		1.25		V
V_{OL}	Output Low Voltage (Pins 10-12-13-16-18-20-21-23) (Pin 9) (Pin 15) (Pins 2-3-4-26-27-28) (Pin 24)	V_{DD} = 4.75V I_{OL} = 1.6mA I_{OL} = 0.2mA I_{OL} = 1mA I_{OL} = 5mA I_{OL} = 2.5mA		 0.2	 0.4 0.4 0.4 1 8	 V V V V V
V_{OH}	Output High Voltage (Pins9-18) (Pin 15)	V_{DD} = 4.75V I_{OH} = – 0.2mA I_{OH} = – 1mA		 V_{DD2} -0.2	 2.4 V_{DD2} -0.4	 V V
$I_{O\ (off)}$	Output Leakage Current (Pins 2-3-4-10-16-20-21-22-23-16-27-28) (Pin 24)	V_{DD} = 4.75V $V_{O\ (off)}$ = 5.25V $V_{O\ (off)}$ = 26V			 10 100	 µA µA
I_{IL}	Input Low Current (Pins 12-13)	V_{DD} = 5.25V, V_{OL} = 0.4V		50	200	µA
I_{OZ}	High Impedance Output Current (Pin 15)	V_O = 0 to V_{DD2}		± 20		nA
I_{DD1}	Supply Current (Pin 6)	V_{DD1} = 5.25V			8	mA
I_{DD2}	Supply Current (Pin 5)	V_{DD2} = 5.25V			30	mA
I_{PP}	Memory Supply Current (Pin 25)	V_{PP} = 26V Write Peak Write Average Erase Peak Erase Average Read Peak Read Average			 40 11 7 4.5 6 2	 mA mA mA mA mA mA

206-05.TBL

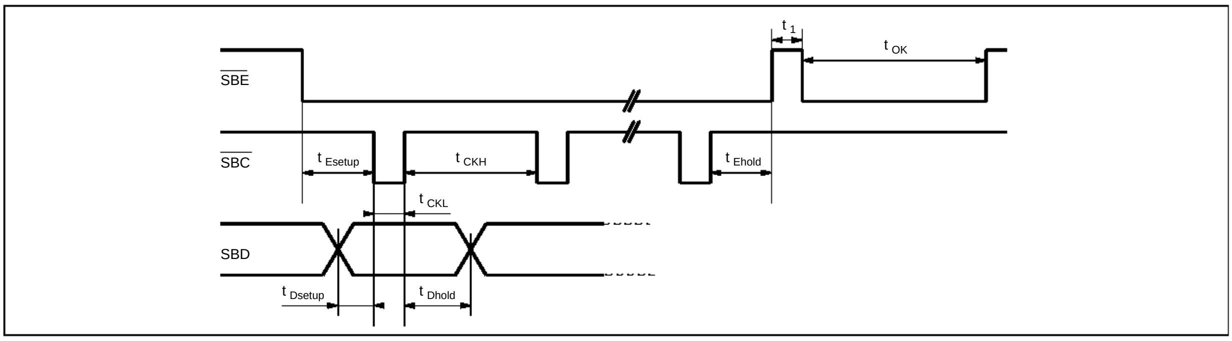
DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Tup.	Max.	Unit
t_{CKL}	$\overline{SBC}$ LOW Time	2		50	µs
t_{CKH}	$\overline{SBC}$ HIGH Time	4			µs
$t_{E\,setup}$	$\overline{SBE}$ Set-up to $\overline{SBC}$ falling edge time	0.5			µs
$t_{E\,hold}$	$\overline{SBE}$ Hold Time from $\overline{SBC}$ rising edge	3			µs
$t_{D\,setup}$	Data Setup Time	1			µs
$t_{D\,hold}$	Data Hold time	1			µs
t_1	Time between $\overline{SBE}$ Rising Edge and OK of Reception			3	µs
t_{OK}	OK of Reception Time		22	26	µs
t_2	Minimum $\overline{SBC}$ Delay Time from OK of Reception	26			µs
t_3	Data Valid Time from OK of Reception		20	25	µs
t_4	Data Valid Time from $\overline{SBC}$ Pulse			4	µs
t_5	Propagation Delay of PMC			0.9	µs

206-06.TBL

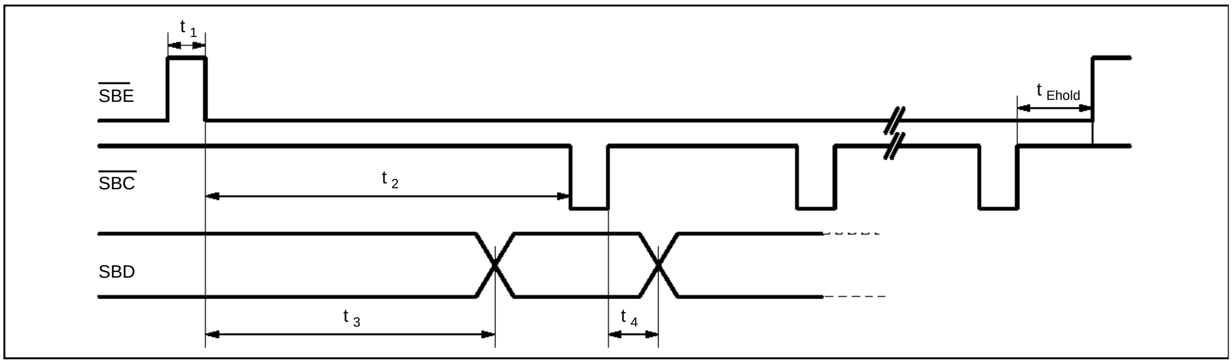
TIMING WAVEFORMS

Figure 7 : Register Load



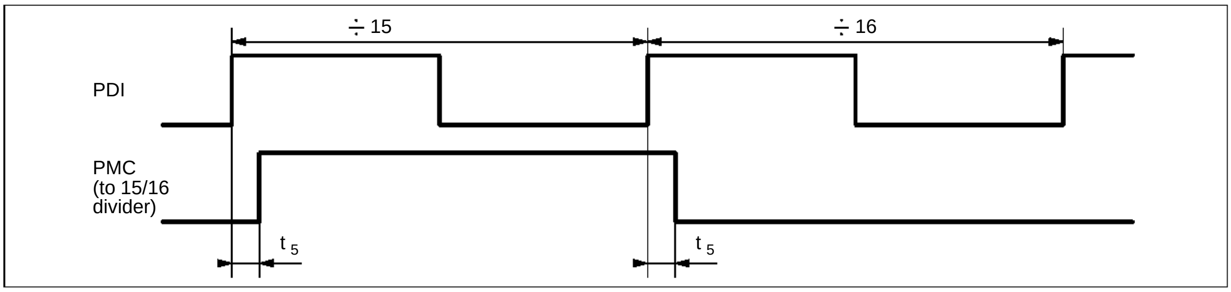
206-09.EPS

Figure 8 : Register Read



206-10.EPS

Figure 9 : Prescaler Modulo Control Timing



206-11.EPS

INPUT AND OUTPUT CONFIGURATIONS

Figure 10 : $\overline{\text{SBC}}$

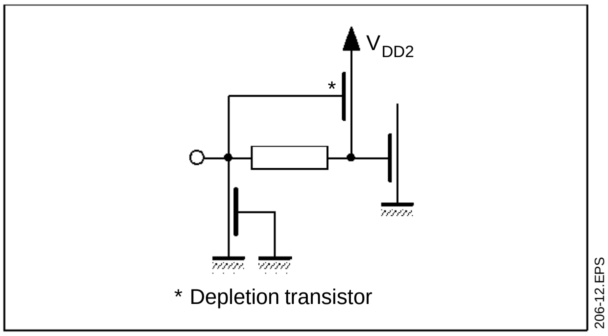


Figure 11 : PDI

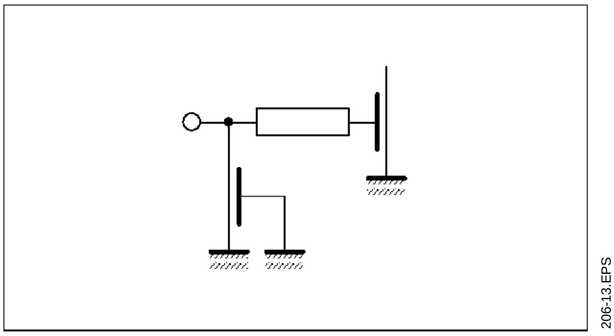


Figure 12 : CLIN

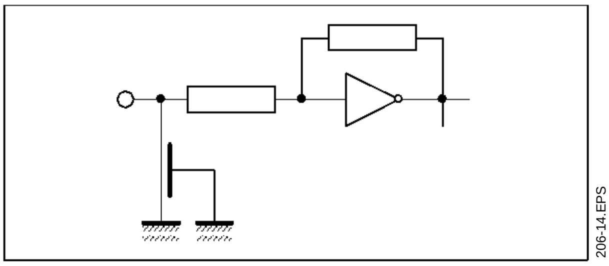


Figure 13 : RCIN

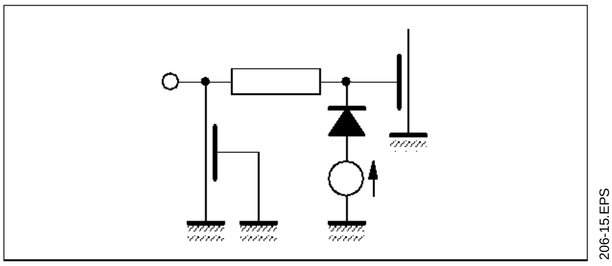


Figure 14 : SBD, $\overline{\text{SBE}}$

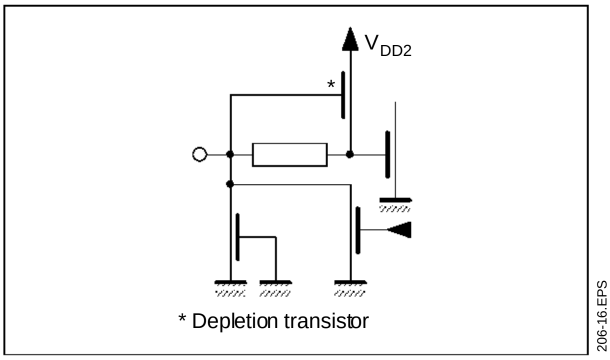


Figure 15 : DA1-DA6, B0-B3, $\overline{\text{OL}}$, RCOUT

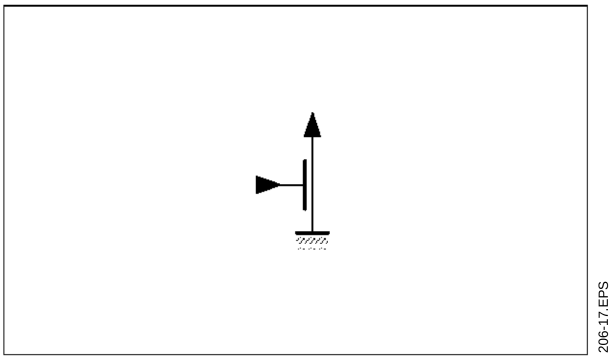


Figure 16 : PCO

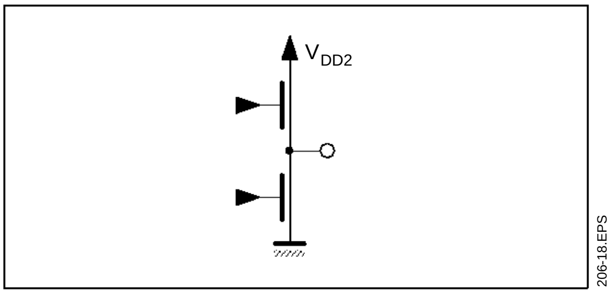
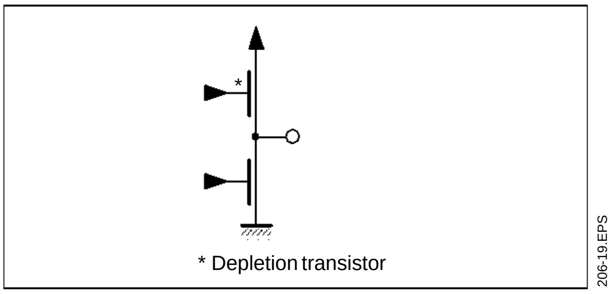
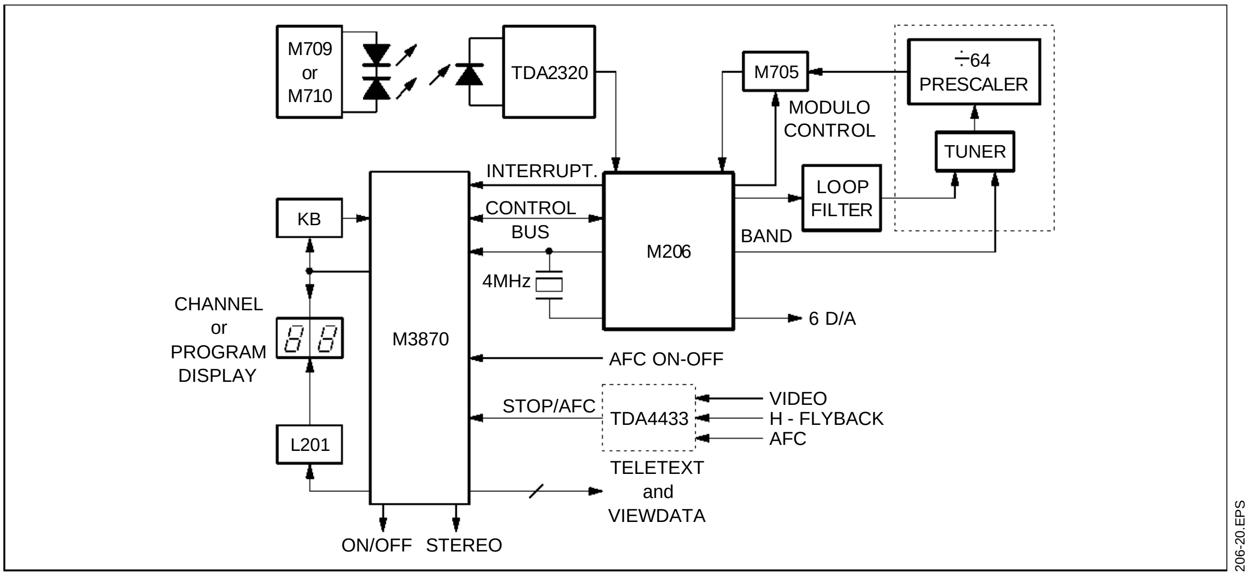


Figure 17 : PMC, CLOUT, CLBUF



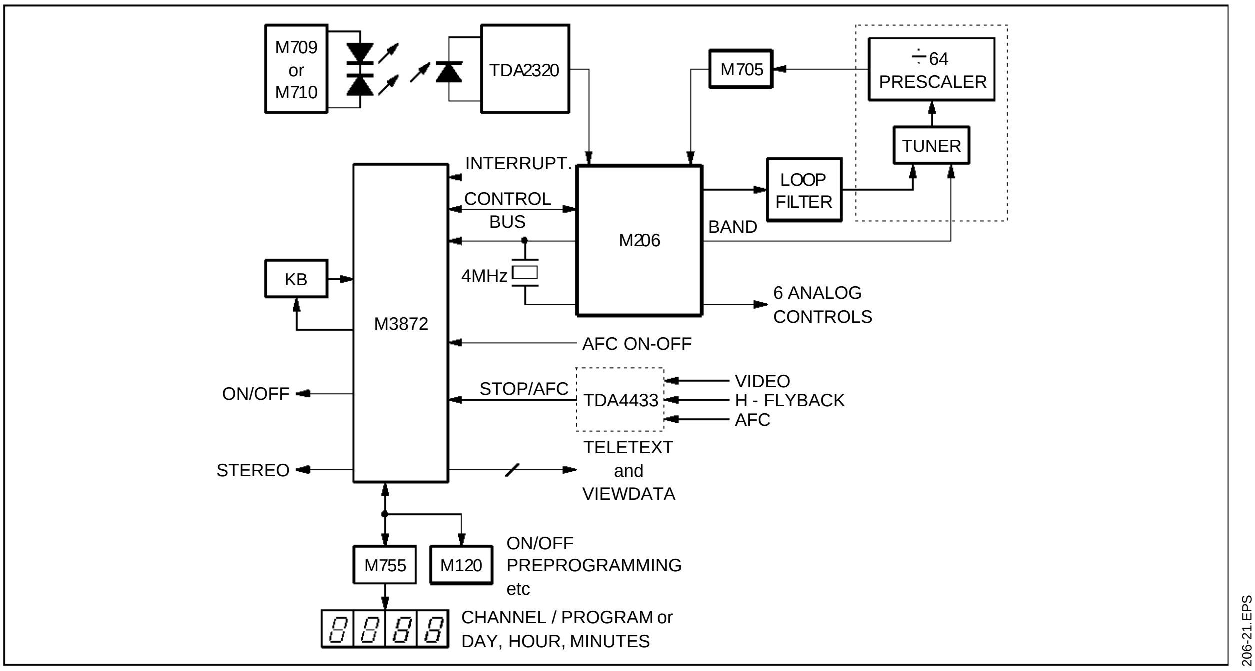
TYPICAL APPLICATIONS

Figure 18 : Remote Controlled TV Frequency Synthetizer



- Remote Control Decoding by Microprocessor.
- 32 Station Non-Volatile Memory or 30 Station
- Memory + Normalized D/A Positions
- Flexible System Operation
- Frequency Synthesis of all Standard and CATV Channels
- Direct Channel Selection
- ± 4MHz Fine Tuning (62.5kHz per Step)
- Automatic Search within Channel (using TDA4433)
- AFC Operation (using TDA4433)
- 6 D/A Converters
- Teletext and Viewdata Data Bus Conversion

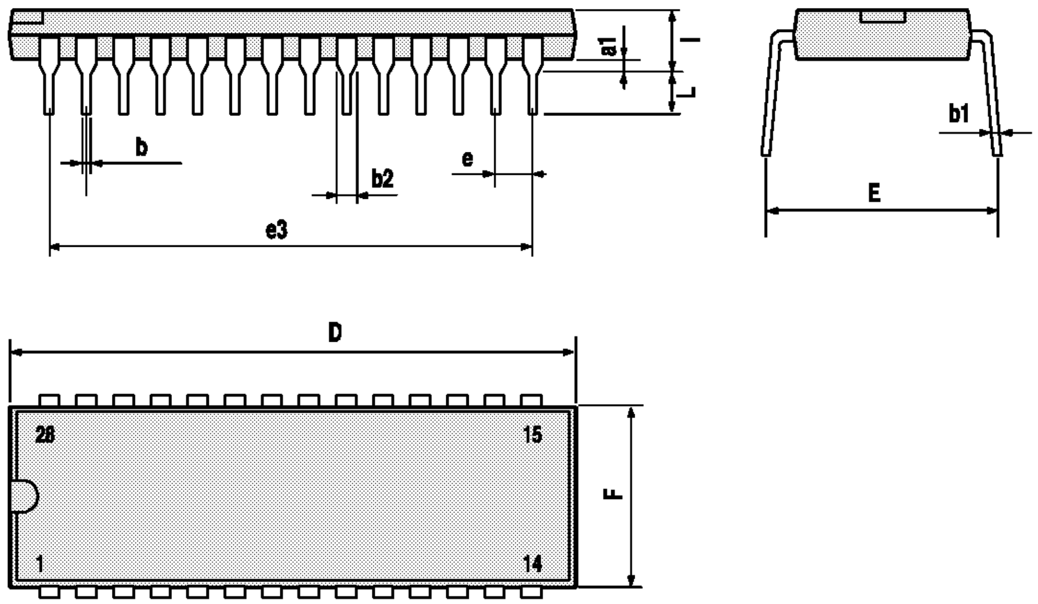
Figure 19 : Remote Controlled TV Frequency Synthetizer and Clock Timer



Frequency Synthesis as described in the Basic Configuration with the addition of :
- Further Station Memory, using M120, 1 K NV MEMORY
- Clock and programmable timer for automatic switch ON/OFF, using M755.

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



PM-DIP28.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP28.TBL